AMENDMENTS

In the Specification

The following is a marked-up version of the specification with the language that is underlined ("___") being added and the language that contains strikethrough ("—") being deleted:

For the paragraph beginning at page 2, line 12:

An ESD incident pulse will propagate through D11 and the base collector junction of T11 and T12 turning on T13, T14 T15 and T16, shunting the ESD current to ground. The circuit has appropriate feedback to maintain the shunted current flow until the ESD even is terminated. The device does offer ESD protection, but there is a large capacitance of approximately .27 pF associated with this prior art design. As previously mentioned, the capacitance comes primarily from the N well ~~300~~ 180 to P substrate 100 junction as well as from the N+ NFET drain 241 and the P substrate 100 junction. This level of capacitance on the input circuit of an RF device can be detrimental to circuit high frequency performance. The invention provides a novel and unique structure and process that provides effective ESD protection while reducing the device capacitance by a nominal order of magnitude to the range of .02 to .03 pF.

For the paragraph beginning on page 6, line 5 to page 7, line 14:

Fig. ~~3~~2 depicts the cross section of the low input capacitance depletion mode SCR with isolate N-channel FET elements. The figure also depicts the parasitic bipolar transistors elements within the structure. The structure is formed as indicated by the flow

description shown in Fig. 4. A N-well 18 is created within the substrate 10. Multiple shallow trench isolation(STI) elements 20, are created within the substrate surface region, which abut the P+ ~~N-well~~ contact region 32, and bridge the N-well 18 to substrate 10. ~~Poly g~~Gate elements 25, 27, are created on the substrate surface. The gate elements have an oxide insulation element and doped poly conductor element. N+ source regions 61, 62 and N+ drain regions are created which in conjunction with the gate elements, form NFET1 and NFET2. Several P+ contact regions 30 are created within the substrate 10 near the NFET source regions 61, 62. Also created is a P+ contact region 32 within the N-well 18. One aspect of the invention is to allow the NFET1 and NFET2 gate elements 25, 27 and drains 41, 42 to be floating electrically to minimize junction capacitance. A first electrical conductor system is created to connect the ~~N-well 18~~ P+ contact region 32 to a first voltage source, typically the active integrated circuit signal input pad 8. At the same time a second electrical conductor system is created which connects NFET1 source 61 and NFET2 source 62 as well as the substrate P+ contacts 30 to a second voltage source, typically ground. A passivation layer is created to protect the ESD protection device from the environment.

The vertical parasitic PNP bipolar transistors T1 and T2 depicted in Fig. 2 are formed from the ~~N-well~~ P+ contact region 32 for the emitters, the N-well region 18 for the base elements, and the P substrate 10 for the collectors. The diode D1 is formed with the anode being the P+ ~~N-well~~ contact regions 32 and the cathode being the N-well 18. The resistors R1 and R2 are representative of the spreading resistance in the N-well area 18. Lateral parasitic NPN bipolar transistors T3 and T4 are formed ~~from~~ with the N+ FET drains 41, 62 for the emitters, the P substrate 10 for the base regions, and the N-well

18 for the collectors. R3 and R4 are representatives of the resistance in the substrate body 10 and are typically in the 200 to 2000 ohms per square range.

A representative electrical schematic of the parasitic bipolar transistors, the NFET elements and the input diode is shown in Fig. ~~4~~3. When an ESD voltage incidence occurs, the charge through the diode D1 turns on the parasitic transistors T1 and T2 that then conduct part of the ESD current to ground. The collector currents flowing through R3 and R4 create a forward bias for transistors T3 and T4, turning them on also. The parasitic bipolar transistors T1 and T3 essentially form a SCR device as do transistors T2 and T4. Once triggered, the ESD current flows until the incident voltage is removed. This multiple parasitic transistor configuration provides additional shunt paths to ground enabling the handling of significant ESD current and affording good ESD protection to the internal active circuits.

For the paragraph beginning on page 8, line 12:

As depicted in Fig. 5D, processing continues with patterning and etching to prepare for the gate oxide deposition. A thermal growth of gate oxide ~~36~~, typically to a thickness of between 50 and 300Å, is placed on the substrate. The gate oxide ~~36~~ is covered by a LPCVD deposition of polysilicon (poly) 36 which is subsequently donor doped to improve conductivity. A LPCVD of a mask oxide 38 is placed over the poly 36, and photoresist patterning is done to prepare of source/drain implantation. A dry etch is performed on the surface layers to provide an opening to the substrate for the source elements 61 and 62, and drain elements 41 and 42 of the NFETs. A donor implant, typically phosphorous(P), with a dosage between 1E14 and 1E17 a/cm^2 and with an

energy of between 10 and 80KeV is performed. This produces source and drain N+ regions with concentrations between 1E19 and 1E21a/cm^3.

For the paragraph beginning on page 9, line 4:

The conductor system 64 for the ~~N well~~ P+ contact region 32 and the conductor system 66 for the N+ NFET source elements 61 and 62 and the P+ substrate contacts 30 are created by a blanket evaporation of a metal, typically aluminum or aluminum doped with 1% silicon. After evaporation any unwanted metal is etched typically with a RIE process after being appropriately patterned. A protective passivation layer 68 is typically deposited SiO_2 doped with boron and phosphorous to form borophosphorus silicate glass. The deposition typically takes place with a temperature between 400 and 500 °C. The deposition is often followed by a densification anneal at a temperature between 700 and 800 °C.